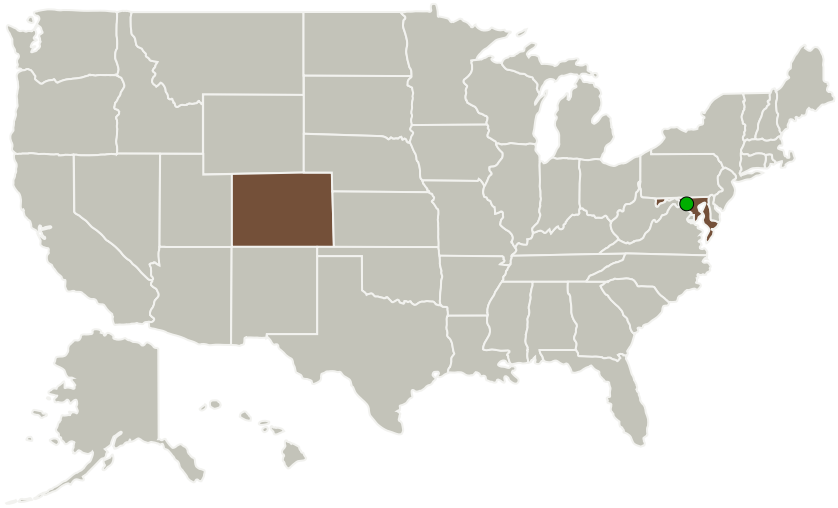
# Radiation Hardened Structured ASIC Platform for Rapid Chip Development for Very High Speed System on a Chip (SoC) and Complex Digital Logic Systems, Phase II

Completed Technology Project (2015 - 2017)

## Project Introduction

Radiation Hardened Application Specific Integrated Circuits (ASICs) provide the highest performance, lowest power and smallest size ICs for Space Missions. To dramatically reduce the development cycle, and reduce cost to tape out, Micro-RDC proposes a Structured ASIC approach. In this methodology, we fix an array of complex logic cells and provide a fixed area array for I/O pads supporting in excess of 400 Complementary Metal-Oxide Semiconductor (CMOS) General Purposes Input/Output (GPIO) pins. In addition, we fix the power grid and the pins associated with power (core and I/O) and ground. Thus, we require only routing in a subset of the metal layers to configure the Structured ASIC for a specific design. This leads to substantial reduction in design and verification time to tape out. Costs are reduced by requiring a subset of mask changes per design. In this work, we will build on Micro-RDC's existing 90nm silicon-proven Radiation Hardened Structured ASIC platform. We will develop a Structured ASIC platform at the 45nm SOI technology node. The objective is to increase clock speeds to hundreds of MHz. Single Event Upset (SEU) immunity is achieved in the sequential logic using Temporal Latch® Technology. We will provide turnkey Register Transfer Language (RTL) to GDSII capability for Radiation Hardened ASICs.

## Primary U.S. Work Locations and Key Partners

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## Table of Contents

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| Organizations Performing Work | Role | Type | Location |
|---|---|---|---|
| Microelectronics Research Development Corporation | Lead Organization | Industry | Colorado Springs, Colorado |
| Goddard Space Flight Center(GSFC) | Supporting Organization | NASA Center | Greenbelt, Maryland |

| Primary U.S. Work Locations | |
|---|---|
| Colorado | Maryland |

## Project Transitions

**June 2015:** Project Start

**September 2017:** Closed out

**Closeout Documentation:**

- Final Summary Chart*(https://techport.nasa.gov/file/137440)*

## Organizational Responsibility

**Responsible Mission Directorate:**

Space Technology Mission Directorate (STMD)

**Lead Organization:**

Microelectronics Research Development Corporation

**Responsible Program:**

Small Business Innovation Research/Small Business Tech Transfer

## Project Management

**Program Director:**

Jason L Kessler

**Program Manager:**

Carlos Torrez

**Principal Investigator:**

Greg Pauls

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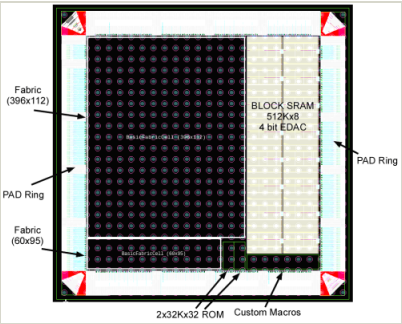
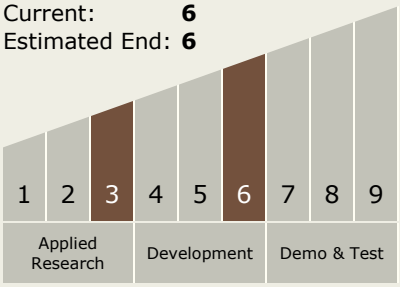
## Images




**Briefing Chart**
Radiation Hardened Structured ASIC Platform for Rapid Chip Development for Very High Speed System on a Chip (SoC) and Complex Digital Logic Systems Briefing Chart
*(https://techport.nasa.gov/image/129252)*

## Technology Maturity (TRL)

Start: **3**
Current: **6**
Estimated End: **6**




## Technology Areas

**Primary:**

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.5 High Performance Field Programmable Gate Arrays

## Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System